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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,576	08/18/2003	Mark S. Birrittella	1376.693US1	3945
21186	7590	01/03/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.			LUU, AN T	
P.O. BOX 2938			ART UNIT	
MINNEAPOLIS, MN 55402			PAPER NUMBER	
			2816	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/643,576

Applicant(s)

BIRRITELLA, MARK S.

Examiner

An T. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8-19-04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “*first and second control signals*” must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

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pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-40 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for “*a first control signal*” and “*a second control signal*”, does not reasonably provide enablement for the above limitations. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims.

In claim 1, the recitation on lines 2-7 calls for “*a first programmable logic circuit to output one of a plurality of variable incremental high logic signals upon receiving a first control signal based on one of a predetermined amount of incremental high signals from a high signal of an input clock signal or to output one of a plurality of variable decremented high logic signals upon receiving a second control signal based on one of a predetermined amount of decremented high signals from the high signal of the input clock signal*”. The above statement is merely a paraphrase of the third paragraph on page 6 of the specification. The specification does not disclose how to achieve a first or second control signal from *on one of a predetermined amount of incremental (decremented) high signals from a high signal of an input clock signal*. Further, figure 1 and 2 do not show that a first logic programmable logic circuit 110 is dependent on the clock input (CLK IN). The first and logic programmable logic circuit 110 and 120 are shown to be dependent on a single input, namely DATA. Therefore, the limitations “*a first control signal*” and “*a second control signal*” in the claim are not supported by the disclosure. Similar reasoning is also applicable for the limitations “*a third control signal*” and “*a fourth control signal*”. Claim 17 has the same problem as that of claim 1.

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As to claim 31, it is rejected for the same reasons as set forth in claim 1 as noted above.

Specifically, lines 3-5 are not supported by the specification.

As to claim 39, similar argument, as noted above, is applicable for limitation “*inputting first and second programming instructions*”.

All other claims are rejected for being dependent on the rejected claims.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation “the predetermined amount of incremental and decremented high signals” of claim 3, line 3, lacks antecedent basis.

The limitation “the plurality of incremental high signals” of claim 4, line 4, lacks antecedent basis.

The limitation “the plurality of decremented high signals” of claim 7, line 4, lacks antecedent basis.

The limitation “the incremented high logic signal or the decremented high logic signal” lacks antecedent basis.

Examiner first believes the inconsistency of reciting terms “*high signal*” and “*high logic signal*” with respect to “*a first control signal*” or “*a second control signal*” in claim 1 create antecedent basis problem for claims 3, 4, 7 and 10 as noted above. Secondly, it is unclear if

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incremented/decremented high logic signal of a second programmable logic circuit is the same as that of *a first programmable logic circuit*. Lastly, the recitation of limitation “*of a second programmable logic circuit*” appears to be incomplete since it has nothing to do with rest of the apparatus as recited in claim 1.

As to claim 17, it is unclear if *incremented/decremented high logic signal of a second edge-triggered circuit* is the same as that of *a first edge-triggered circuit*. Further the recitation of limitation “*of a second edge-triggered circuit*” appears to be incomplete since it has nothing to do with rest of the apparatus of the claim.

As to claim 31, it has the same problems as that of claim 17. Therefore, it is rejected for the same reasons as set forth above.

As to claims 2, 5, 6, 8,9, 11-16, 18-30 and 32-38 are rejected for being dependent on the rejected claims as noted above.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

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international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1, 17, 31-34 and 38-39, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by the Kwak reference (U.S. Patent 6,677,792).

Kwak discloses in figures 1 and 2 an apparatus comprising a first programmable logic circuit (121 and 123) to output incremental high logic signals upon receiving a first control signal (output of 150) based on one of a predetermined amount of incremental high signals from a high logic signal of an input clock signal (EXT-CLK) or to output one decremented high logic signals upon receiving a second control signal (output 160) based on one of a predetermined amount of decremented high signals from the high logic signals of the input clock signal;

a second programmable logic circuit 140 to output an incremented high logic signal upon receiving a third control signal (output of 130);

a positive variable duty cycle adjust circuit 122 (and see chart in fig. 2) to couple to an input clock terminal (EXT-CLK) to receive the input clock signal and to output one of a plurality of incremented duty cycle clock signals having an incremented high signal from the high logic signal of the input clock signal as a function of the first control signal;

a negative variable duty cycle adjust circuit 124 (and see chart in fig. 2) to couple to couple to the EXT-CLK to receive the input clock signal and to output one of a plurality of decremented duty cycle clock signals having a decremented high signal from

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the high logic signal of the input clock signal as a function of the second control signal;
and

an output module 130 to couple to an output clock terminal (INT-CLK) to output an adjusted clock signal having one of the plurality of incremented or decremented duty cycle clock signals as a function of the incremented or decremented high logic signal, respectively as required by claim 1.

As to claim 17, the scope of claim is similar to that of claim 1. Therefore, it is rejected for the same reason set forth above. It is noted that “programmable logic circuit” is interpreted as “edge-triggered circuit”.

As to claims 31 and 39, they are rejected for reciting method/step derived from an apparatus of claim 17. Therefore, they are rejected for the same reasons set forth above.

As to claim 32, figure 8 and its associated description in col. 10 disclose method of multiplexing the outputted incremented or decremented duty cycle adjusted clock signal.

As to claims 33 and 34, figure 2 discloses EXT_CLK being a logic signal of a pulse type waveform that switches from low to high and then from high to low with a fixed repetition pattern in time and the pulse type waveform comprises high and low signals in each clock cycle.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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9. Claims 2, 18, 37-38 and 40, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Kwak reference (U.S. Patent 6,677,792) in view of the Martin reference (U.S. Patent 6,040,726).

Kwak discloses all the claimed invention except for teaching a clock signal input generated by an oscillator as required by claim 2.

Martin discloses in figure 1 and col. 1, lines 29-31, an apparatus having a clock signal input generated by an oscillator as required by claim 2.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Martin into that of Kwak since an oscillator is well known to provide a clock signal.

A skilled artisan in the art would have been motivated to use an oscillator for generating a clock signal since it is suitable in an analog environment.

Further, it is obvious that a clock signal comprising a stream of pulses having a particular repetition pattern in time of HIGH and LOW levels.

As to claims 18, 37 and 40, the scopes of these claims are similar to that of claim 2. Therefore, they are rejected for the same reason set forth above.

As to claim 38, column 1, line 48, discloses the input clock having fifty-percent duty cycle.

10. Claims 35 and 36, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over the Kwak reference (U.S. Patent 6,677,792) in view of the Wu et al reference (U.S. Patent 6,100,736).

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Kwak discloses all the claimed invention except for teaching specific steps of “*storing the first and second programmed instruction in associated memory elements of the integrated circuit wherein the memory elements comprising devices selected from the group consisting of registers and flip-flop circuits*” as required by claims 35-36.

Wu discloses in figure 3 (including an associated description in column 4) and figure 5B an apparatus to carry out method/step of *storing the first (CTRL 39) and second (CTRL 38) programmed instruction in associated memory elements (corresponding shift register as shown)* as required by the claims.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Wu et al into that of Kwak since Kwak discloses circuitry and methods with respect to general components having a preferred embodiments which can be implemented in many different ways.

A skilled artisan would have been motivated to incorporate the teachings of Wu et al since it provides a stable output after a few clock cycles without additional external control and consumes less power to operate.

Allowable Subject Matter

11. Claims 3-16 and 19-30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to disclose an apparatus comprising elements being configured as recited

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in claims. Specifically, none of the prior art teaches or fairly suggests, among other things, the programmable logic circuit having the output of the inverter coupling to the positive variable duty cycle adjust circuit and the negative variable duty cycle adjust circuit as required by claims 3, 19, 21, 23 and 25.


Conclusion

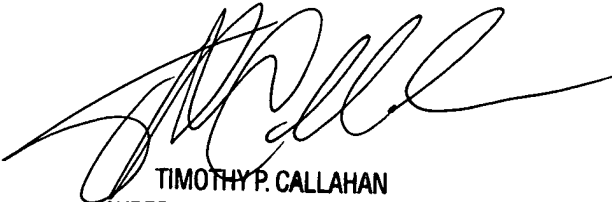
13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
12-21-04 


TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800